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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,103	11/19/2003	Rong Yin	03-C-058	8891

7590 06/11/2007

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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	**PAPER NUMBER**
2836	

MAIL DATE	DELIVERY MODE
06/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,103	YIN, RONG	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-3,8-9, 15-23* is/are rejected.

7)☒ Claim(s) *4-7,10-14 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amendments filed on 04/23/2007.

2. The indicated allowability of claims16-20 is withdrawn in view of Bullmore (US 2004/0051643).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 15-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Bullmore (2004/0051643).

With respect to claim 1 Bullmore discloses a circuit for monitoring the state of at least one switch (monitoring system fig. 2), comprising: a first monitoring circuit (monitoring devices 10, 20 and 30), couple to a switch (monitoring devices are couple to switches SWA, SWB, SWC), the switch being one of a normally-open switch or a normally-closed switch, comprising: a normally-open detection circuit coupled to a first

terminal of the switch (electrical circuits A, B and C are configured to detect a normally-open or a normally-closed state of a switch by changing a resistance of the circuit, page 3 paragraph (0040), the detection circuit is couple to the switch as shown in the figures) for detecting when the switch, if configured as a normally-open switch, closes and generating a first signal based on the detection; and a normally-closed detection circuit also coupled to the first terminal of the switch for detecting when the switch, if configured as a normally-closed switch, opens and generating a second signal based on the detection (electrical circuits A, B and C, can detect a close or open condition of a switch by a change in resistance in the circuit, thus the electrical circuits function as a normally-open detection circuit and as a normally-closed detection circuit, page 3 paragraph (0042), page 4 paragraph (0052)); and a configuring circuit (centralized SMS control unit 5), coupled to the first monitoring circuit, for configuring the first monitoring circuit to utilize the normally-open detection circuit and disable the normally- closed detection circuit if the switch is a normally-open switch or alternatively utilize the normally-closed detection circuit and disable the normally-open detection circuit if the switch is a normally-closed switch (as shown in figure 2 the monitoring devices communicate with the control unit 5). Paragraph (0006) discloses how the normally open circuit and the normally close circuit work.

With respect to claim 15 Bullmore discloses the circuit of claim 1, wherein the circuit further comprises: a second monitoring circuit (monitoring devices 20 and 30), coupled to a second switch (SWB, SWC), the second switch being one of a normally-open switch or a normally-closed switch comprising: a second normally-open detection

circuit coupled to a first terminal of the second switch for detecting when the second switch, if configured as a normally-open switch, closes and generating a third signal based on the detection; and a second normally-closed detection circuit also couple to the first terminal of the switch for detecting when the second switch, if configured as a normally-closed Switch, opens and generating a fourth signal based on the detection (electrical circuits B and C are configured to detect a normally-open or a normally-closed state of second and third switches by changing a resistance of the circuit, page 3 paragraph (0040)), wherein the configuring circuit is coupled to the second monitoring circuit, for configuring the second monitoring circuit to utilize the second normally-open detection circuit and disable the second normally-closed detection circuit if the switch is a normally-open switch or alternatively utilize the second normally-closed detection circuit and disable the normally-open detection circuit if the second switch is a normally-closed switch (as shown in figure 2 the monitoring devices communicate with the control unit 5 providing a second and third signals).

With respect to claim 16,20 Bullmore discloses a method for detecting the state of at least one switch using a circuit, comprising: configuring a circuit, coupled to a switch, based on whether the switch is a normally-open switch or a normally-closed switch (as shown in figure 2 the monitoring devices communicate with the centralized SMS control unit 5, the switches (SWA, SWB, SWC) can be a normally-open or a normally-closed switch, paragraph 0052), wherein configuring the circuit comprises: activating a normally-open detection circuit and deactivating a normally-closed detection circuit if the switch is a normally-open switch; and activating the normally-closed

detection circuit and deactivating the normally-open detection circuit if the switch is a normally-closed switch; detecting, by the activated one of the normally-open detection circuit and the normally-closed detection circuit, the switch changing states; and generating a signal indicative of the detection. Paragraph (0006) discloses how the normally open circuit and the normally close circuit works, and since the switch can be either normally-open or a normally-closed switch, depending on the resistance detected the state of the switch is detected.

With respect to claim 17 Bullmore discloses the method of claim 16, wherein the step of configuring comprises configuring the circuit to relatively weakly pull a terminal of the switch towards a voltage representative of one of a logic high state and a logic low state. The switch can be a normally-open or normally-closed switch, thus depending on the requirements the switch is either open or closed and EOL is detected representing a low or high state.

With respect to claim 18-19 Bullmore discloses the method of claim 17, wherein the step of configuring comprises activating transistors to couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state, and wherein the step of configuring comprises occasionally activating at least one transistor to occasionally couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state . Figure 2 shows the switches connected to resistors R1 and R2, representing one of a low or high logic states.

With respect to claim 21 Bullmore discloses a system, comprising: a switch having a first conduction terminal and a second conduction terminal (SWA, SWB and SWC have a first and conduction terminal as shown in figure 2), the switch being one of a normally-open switch or a normally-closed switch (paragraph 0052, the switches could be a normally-open or a normally-closed switch); a first circuit coupled to the first conduction terminal of the switch for detecting the switch opening and generating if activated a signal indicative of that detection; a second circuit coupled to the first conduction terminal of the switch for detecting the switch closing (monitoring devices 10, 20 and 30 act as the first and second circuit, because the monitoring devices are able to check a switch opening or closing) and generating if activated a signal indicative of that detection; a third circuit (centralized SMS control unit 5) coupled to the first circuit and the second circuit for configuring the first and second circuits by activating the first circuit and deactivating the second circuit if the switch is a normally-closed switch and deactivating the first circuit and activating the second circuit if the switch is a normally-open switch (control unit 5 controls the operation of each of the switches by controlling the monitoring devices, thus the control unit based on the state of the switches is able to control the monitoring devices and the switches to change state). Furthermore Paragraph (0006) discloses how the normally open circuit and the normally close circuit work.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-3, 8-9,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bullmore (2004/0051643) in view of Youssef (US 6,861,955).

With respect to claim 2 Bullmore discloses the circuit of claim 1, except for pulling the first terminal of the switch to a voltage representative of one of a logic high state and a logic low state.

Youssef discloses in Figure 2 a First circuit 12 (third circuit) for detecting the opening and closing of switch 20 and for pulling terminal 21 of switch 20 to logic low (ground) or logic high (power supply), Column 3 lines 21-23, lines 27-29. It would have been obvious at the time the invention was made to have combined the Bullmore circuit for detecting the opening and closing of a switch with Youssef circuit invention for pulling a terminal of the switch to a logic high state and a logic low state.

The suggestion or motivation for doing so would have been to improve the reliability and operability of the switch and to make sure the switch and the circuits are giving the right output based on the detection of the switch.

With respect to claim 3 Bullmore in view of Youssef discloses the circuit of claim 2, wherein the closed-to-open circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state Youssef (Column 3 lines 21-23, lines 27-29).

With respect to claim 8 Bullmore in view of Youssef discloses the circuit of claim 1, wherein the normally-open detection circuit includes a open-to-closed circuit for

detecting whether the switch changes from an open state to a closed state and for relatively weakly pulling the first terminal of the switch towards a voltage representative of one of a logic high state and a logic low state. As discussed in claim 2 above Youssef discloses a first circuit 12 for detecting the opening and closing of switch 20 and for pulling a terminal to ground or to a power supply. For the purpose of improving the reliability and operability of the switch and to make sure the switch and the circuits are giving the right output based on the detection state of the switch.

With respect to claim 9 Bullmore in view of Youssef discloses the circuit of claim 8, wherein the open-to-closed circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state (Column 3 lines 21- 23, lines 27-29).

With respect to claim 22 Bullmore discloses the system of claim 21. However, Bullmore does not disclose expressly that the activated first/second circuit is configurable to one of: selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic high state, or selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic low state. As disclosed by Youssef in one of the claims above, Figure 2 shows a circuit 12 for detecting the opening and closing of switch 20 and for pulling terminal 21 of switch 20 to logic low (ground) or logic high (power supply), Column 3 lines 21-23, lines 27-29.

It would have been obvious at the time the invention was made to have combined the Bullmore circuit for detecting the opening and closing of a switch with

Youssef circuit invention for pulling a terminal of the switch to a logic high state and a logic low state.

The suggestion or motivation for doing so would have been to improve the reliability and operability of the switch and to make sure the switch and the circuits are giving the right output based on the detection of the switch.

With respect to claim 23 Bullmore in view of Youssef discloses the system of claim 22, except for activated circuit selectively weakly pulls the first terminal of the switch towards a certain logic state, relative to a drive strength of the switch to pull the first terminal thereof towards a different logic state. Youssef (Column 3 lines 12-15, 21-23 and lines 27-29).

Allowable Subject Matter

7. Claims 4-7, 10-14, 24-26 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 4 is allowable over the prior art of record, because the prior art of record does not suggests that "a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source; a second transistor coupled between the first terminal of the at least one resistive element and the first terminal of the switch; a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source, and a fourth transistor couple

between the second terminal of the at least one resistive element and the first terminal of the switch".

9. Claims 5-7 are allowable because they depend on allowable claims.

10. Claim 10 is allowable over the prior art of record, because the prior art of record does not suggests that "the third circuit comprises at least one first transistor coupled between a high reference voltage level and the first terminal of the switch, at least one second transistor coupled between a low reference voltage level and the first terminal of the switch, and control logic for generating at least one control signal having a value indicative of a configuration of the third circuit, a control terminal of each of the at least one first transistor and the at least one second transistor having a value based upon the value of the at least one control signal".

11. Claims 11-14 are allowable because they depend on allowable claims.

12. Claim 24 is allowable over the prior all: of record, because the prior art of record does not suggests that "a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source; a second transistor coupled between the first terminal of the at least one resistive element and the first conduction terminal of the switch; a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source; and a fourth transistor coupled between the first conduction terminal of the switch and the second terminal of the at least one resistive element".

13. Claims 25-26 are allowable because they depend on allowable claims.

Response to Arguments

14. Applicant's arguments filed 04/23/2007 have been fully considered but they are not persuasive.

With respect to claim 1 Bullmore discloses that a state of the switch is detected based on if the switch is a normally-closed or a normally-open switch (EOL resistance).

With respect to claim 21 as disclosed on paragraph (0006) an open state is detected when the line resistance is R1 plus R2, and a closed state is detected when the line resistance is R1. Bullmore discloses that the switches can be either of an open or closed configuration paragraph 0052.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Amaya whose telephone number is (571) 272-8941. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CA

6/7/07

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